WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a monolithic substrate;

a NOR array of memory cells configured upon and within the substrate, wherein each NOR array memory cell includes a single NOR transistor having a NOR transistor source node coupled to a power supply and a NOR transistor drain node coupled to a first bit line; and

a NAND array of memory cells configured upon and within the substrate, wherein each NAND array memory cell includes a single NAND transistor having a NAND transistor source node coupled to a second bit line and a NAND transistor drain node coupled to a NAND transistor source node of another NAND transistor within another cell of the NAND array of memory cells.

2. The semiconductor memory device as recited in claim 1, wherein the monolithic substrate comprises single crystalline silicon.

3. The semiconductor memory device as recited in claim 1, wherein the monolithic substrate comprises gallium arsenide.

4. The semiconductor memory device as recited in claim 1, wherein the NOR array is configured upon a first portion of the monolithic substrate spaced from the NAND array configured upon a second portion of the monolithic substrate.

5. The semiconductor memory device as recited in claim 1, wherein the NOR transistor and the NAND transistor each comprise a floating gate.

6. The semiconductor memory device as recited in claim 5, wherein the floating gate is dielectrically spaced between the substrate and a corresponding control gate.

7. The semiconductor memory device as recited in claim 5, wherein the floating gate is adapted for receiving electrons during a time in which the floating gate is programmed.

8. The semiconductor memory device as recited in claim 1, further comprising:

an address decoder;

a NOR array row decoder;

a NOR array column decoder; and

wherein the address decoder, the NOR array row decoder, and the NOR array column decoder are adapted for reading data from, programming data into and erasing data within the NOR array if an incoming address on a memory bus decoded by the address decoder is targeted for the NOR array.

9. The semiconductor memory device as recited in claim 8, wherein the address decoder, the NOR array row decoder and the NOR array column decoder are configured upon and within the substrate.

10. The semiconductor memory device as recited in claim 1, further comprising

an address decoder;

a page and block controller;

a data register;

a NAND array row decoder;

a NAND array column decoder;

wherein the address decoder, the NAND array row decoder, and the NAND array column decoder are adapted for reading data from, programming data into and erasing data within the NAND array if an incoming address on a memory bus decoded by the address decoder is targeted for the NAND array; and

wherein the data register stores pages of data transferred between a memory bus and the NAND array during different stages of transfer depending on the status of a command latch enable (CLE) signal, an address latch enable (ALE) signal, a write enable (WE) signal, and a read enable (RE) signal produced from the page and block controller.

11. The semiconductor memory device as recited in claim 10, wherein the address decoder, the page and block controller, the data register, the NAND array row decoder and the NAND array column decoder are configured upon and within the substrate.

12. A semiconductor memory device, comprising:

a NOR array of memory cells;

a NOR array of row and column decoders for selecting at least one memory cell of the NOR array of memory cells;

a NAND array of memory cells;

a NAND array of row and column decoders for selecting a plurality of the NAND array of memory cells;

a page and block controller coupled to the NAND array row and column decoders for controlling the NAND array and column decoders;

an address decoder configured to receive an address from a memory bus and route the address to either (i) the NOR array row and column decoders or (ii) the page and block controller depending on whether the address is to information stored in the NOR array of memory cells or the NAND array of memory cells; and

wherein the NOR array of memory cells, the NOR array of row and column decoders, the NAND array of memory cells, the NAND array of row and column decoders, the page and block controller and the address decoder are configured as part of an integrated circuit.

13. The semiconductor memory device as recited in claim 12, wherein the integrated circuit is a semiconductor die.

14. The semiconductor memory device as recited in claim 12, wherein the at least one memory cell of the NOR array of memory cells is a byte of eight NOR array of memory cells.

15. The semiconductor memory device as recited in claim 12, further comprising a data register configured as part of the integrated circuit for receiving data transferred between a memory bus and the NAND array of memory cells during different stages of transfer depending on the status of a command latch enable (CLE) signal, an address latch enable (ALE) signal, a write enable (WE) signal, and a read enable (RE) signal produced from the page and block controller.

16. The semiconductor memory device as recited in claim 15, wherein the plurality of the NAND array of memory cells is a page of at least 528 bytes of eight NAND array of memory cells during times when the RE signal or WE signal is active.

17. The semiconductor memory device as recited in claim 16, wherein the plurality of NAND array of memory cells is a block of at least 32 pages during times when the RE signal and WE signal are inactive.

18. A method for transferring data into and from an integrated circuit semiconductor memory device, comprising:

decoding an address on a memory bus external to the semiconductor memory device as targeting either code stored in a NOR array of memory cells or in a NAND array of memory cells, both of which are configured upon the integrated circuit semiconductor memory device;

decoding a read, program or erase command on the memory bus to perform a read operation, a program operation or an erase operation on the NOR array if said decoding produces a target in the NOR array of memory cells; and

converting a read, program or erase command on the memory bus to a read enable (RE), write enable (WE) , command latch enable (CLE), and address latch enable (ALE) command and, depending on the status of RE, WE, CLE and ALE, performing a read operation, a program operation, or an erase operation on pages or blocks of the NAND array of memory cells.

19. The method as recited in claim 18, wherein said converting occurs within a page and block controller configured upon the integrated circuit semiconductor memory device.

20. The method as recited in claim 18, wherein said decoding the address comprises decoding an address range of boot code within the NOR array or look-up tables, character generators, or micro-control code within the NAND array.